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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,466	11/24/2003	Anthony Correale JR.	YOR920030373US1	4073

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,466	CORREALE ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 3/29/06.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 19-30 is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Acknowledgement

Receipt is acknowledged of the Amendment filed March 29, 2006.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-9, 12-15, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Foss (US 4,786,830).

Regarding claim 1, Foss discloses, in Fig. 2, a level converter (the recitation that, "for interfacing circuits in the same integrated circuit (IC) as said level converter and supplied by different supply voltages" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951)) and supplied by different supply voltages, said level converter comprising:

a first buffer (20) receiving an input (21), said first buffer being connected between a virtual supply (25) and a supply return (Vss);

a second buffer (30) receiving an output (24) of said first buffer, connected between a first supply (Vcc) and said supply return (Vss); and

a supply select (6, 9) between said first supply and said virtual supply, said supply select receiving an output (26) from said second buffer and selectively passing a first supply voltage

(Vdd) on said first supply or a reduced supply voltage (Vcc-voltage drop across 6; col. 3, lines 57+) to said virtual supply responsive to said output (26) from said second buffer, said reduced supply voltage being such that standby power is eliminated (col. 4, lines 10+) in said first buffer when said input is high.

Regarding claim 2, Foss discloses, in Fig. 2, that said second buffer is an inverter (col. 3, lines 11+).

Regarding claim 3, Foss discloses, in Fig. 2, that said supply select is a supply switch (9) in parallel with at least one diode (6), both connected between said first supply and said virtual supply.

Regarding claim 4, Foss discloses, in Fig. 2, said supply switch (9) is a field effect transistor (FET)(col. 3, lines 55+) gated by said output (26) of said second buffer and said at least one diode is a diode connected FET (6).

Regarding claim 5, Foss discloses, in Fig. 2, that said supply switch FET is a P-type FET (PFET)(col. 3, lines 55+) and said at least one diode connected FET an N-type FET (NFET) diode (see 6).

Regarding claim 7, Foss discloses, in Fig. 2, that said second buffer is a CMOS inverter (col. 3, lines 9 and 21+).

Regarding claim 8, Foss discloses, in Fig. 2, that said first buffer is a CMOS inverter (col. 3, lines 9 and 21+).

Regarding claim 9, Foss discloses, in Fig. 2, that said first buffer is a logic gate (col. 3, lines 21+).

Regarding claim 12, Foss discloses, in Fig. 2, a voltage level converter circuit comprising:

a first inverter (20) with a first inverter input (21) connected to an output of a first circuit (at least 2, 4) on the same integrated circuit (IC) as said first inverter, a first inverter output (24), a first inverter ground (Vss) connected to a circuit ground (Vss), and a first inverter voltage supply (25);

a threshold drop element (6) connected between a circuit high voltage supply (Vddh) (Vcc) and the first inverter voltage supply (25);

a second inverter (30) with a second inverter input connected to the first inverter output (24) connected to an input of a second circuit (3, 12) on the same integrated circuit (IC) as said second inverter, a second inverter output (26), a second inverter ground connected to the circuit ground (Vss), and a second inverter voltage supply connected to Vddh (Vcc); and

a voltage feedback element (9) connected between Vddh (Vcc) and the first inverter voltage supply (25), the voltage feedback element having an input connected to the second inverter output (26), wherein when the second inverter output is low, the voltage feedback element causes the first inverter voltage supply to approach Vddh (since 9 turns ON) and making the first inverter output approach Vddh thereby eliminating a standby power in the second inverter (col. 4, lines 10+), and wherein when the second inverter output is high, standby power is substantially eliminated in the first inverter (col. 4, lines 10+).

Regarding claim 13, Foss discloses, in Fig. 2, that the threshold drop element (6) provides the first inverter voltage supply with a lower voltage than the circuit high voltage supply (col. 4, lines 28+) when the first inverter input is high (21).

Regarding claim 14, Foss discloses, in Fig. 2, that the threshold drop element is at least one transistor (6).

Regarding claim 15, Foss discloses, in Fig. 2, that the transistor is a field effect transistor (FET) (6).

Regarding claim 18, Foss discloses, in Fig. 2, that the threshold drop element is a diode (6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foss.

Regarding claims 6 and 16 Foss discloses all the features of the claimed invention as discussed above but does not disclose that the at least one diode connected NFET is a plurality or a pair of series connected NFET diodes.

However, it is well known in the art that when more voltage drop is desired, more diodes can be connected in series. Therefore, it would have been obvious at the time the invention was made to an ordinary skilled in the art to have added more well known NFET diode(s) in series with NFET diode (6) of Foss in order to provide more voltage drops.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Foss in view of Feller (EP 0 125 733 A1).

Foss discloses all the features of the claimed invention as discussed above but does not disclose that the first buffer is a NAND gate.

Feller discloses that the first buffer 10 can be any complementary FET arrangement including NAND gate (page 7, lines 16+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the first buffer of Foss with the NAND gate as taught by Feller in order to use another function of complement FET arrangement.

Claims 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foss in view of Kao ("Dual Threshold Voltage Domino Logic", Sept. 1999).

Regarding claim 11, Foss discloses all the features of the claimed invention as discussed above but does not disclose that the output CMOS inverter includes an NFET having a threshold higher than other NFETs.

Kao discloses an output CMOS inverter (I1 in Fig. 1) with an NFET having a threshold higher than other NFETs for reducing leakage currents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the CMOS inverter of Foss with the NFET having a threshold higher than other NFETs as taught by Kao in order to improve reducing leakage or standby currents.

Regarding claim 17, Foss discloses all the features of the claimed invention as discussed above but does not disclose that the FET is a high threshold voltage FET.

Kao discloses dual threshold devices comprising high threshold voltage FET (Pre-charge PMOS parallel with P1 in Fig. 1) for reducing leakage currents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have provided the FET (6) of Foss with the high threshold voltage FET as taught by Kao in order to improve reducing leakage or standby currents.

Response to Arguments

Applicant's arguments filed March 29, 2006, regarding claims 1-18 have been fully considered but they are not deemed to be persuasive.

Regarding claim 1, applicant argues on page 8 that the recitation, "circuits in the same integrated circuit (IC) as said level converter and supplied by different supply voltage" is neither taught nor suggested by the Foss I/O circuit or by any reference of record. However, the recitation that, "for interfacing circuits in the same integrated circuit (IC) as said level converter and supplied by different supply voltages" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

Regarding claim 12, applicant argues on pages 8 and 9 that the recitation, "first inverter with a first inverter input connected to an output of a first circuit on the same integrated circuit (IC) as said first inverter," and "a second inverter output connected to an input of a second circuit on the same integrated circuit (IC) as said second inverter" is neither taught nor suggested by the

Foss I/O circuit or by any reference of record. However, Foss teaches that "a first inverter (20) with a first inverter input (21) connected to an output of a first circuit (at least 2, 4) on the same integrated circuit (IC) as said first inverter"; and "a second inverter (30) with a second inverter input connected to the first inverter output (24) connected to an input of a second circuit (3, 12) on the same integrated circuit (IC) as said second inverter" as discussed above.

Therefore, rejection of claims 1-18 are maintained as discussed above.

Allowable Subject Matter

Claims 19-30 are allowable over the prior art of the record.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Foss, taken alone or in combination of other references, does not teach or fairly suggest an integrated circuit comprising, among other things, at least one low voltage island in at least one of said plurality of circuit rows, circuit elements in each said at least one low voltage island being powered by a low voltage (Vddl) supply, as set forth in the claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

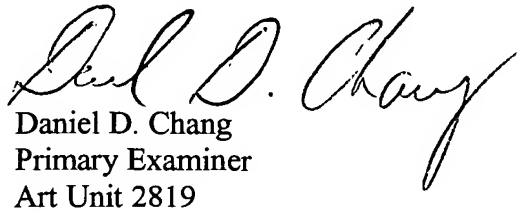
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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